CLAIMS

1. An apparatus comprising:

a processor configured to operate at a first data rate in response to a first clock signal;

an interface circuit configured to (i) operate in response to the first clock signal, and (ii) convert data received from said processor over a system bus from said first data rate to a second data rate; and

a memory (i) coupled to said interface circuit and (ii) configured to present/receive data to/from said system bus at said second data rate.

2. The apparatus according to claim 1, wherein said first clock signal and said second clock signal are independently generated.

3. The apparatus according to claim 1, wherein said second clock signal is generated in response to said first clock signal.

4. The apparatus according to claim 1, wherein said interface circuit comprises a state machine configured to control the conversion between said first and said second data rate.

5. The apparatus according to claim 1, wherein said apparatus provides paging to said memory.

6. The apparatus according to claim 1, wherein said processor comprises (i) a central processing unit (CPU) and a bus interface unit, wherein said CPU communicates with said system bus through said bus interface unit.

7. The apparatus according to claim 1, wherein said interface further comprises a bus interface, wherein said state machine is configured to communicate with said system bus through said bus interface unit.

8. The apparatus according to claim 1, wherein said interface provides paging to said memory.

9. The apparatus according to claim 1, wherein said interface is configured to minimize access requests to said memory.

10. An apparatus comprising:

processor means for operating at a first data rate in response to a first clock signal;

interface means for (i) operating in response to the first clock signal, and (ii) converting data received from said processor means over a system bus from said first data rate to a second data rate; and

memory means for (i) coupling said interface circuit and (ii) presenting data to/from said system bus at said second data rate.

11. A method for paging to a memory comprising the steps of:

(A) operating a processor at a first data rate in response to a first clock signal;

(B) operating an interface circuit in response to a first clock signal;

(C) converting data received from said processor over a system bus from said first data rate to a second data rate; and

(D) operating a memory coupled to said interface circuit and for presenting/receiving data to/from said system bus at said second data rate.